PVP 14

Code: EC6T1

III B.Tech-II Semester–Regular/Supplementary Examinations–March 2018

VLSI DESIGN

(ELECTRONICS & COMMUNICATION ENGINEERING)

Duration: 3 hours Max. Marks: 70

PART – A

Answer *all* the questions. All questions carry equal marks

11x 2 = 22 M

1. a) Give the basic process of IC Fabrication.
   b) What is figure of Merit of MOS transistor?
   c) Define fanout of a logic gate.
   d) What are the two types of layout design rules?
   e) Differentiate between constant field scaling and constant voltage scaling.
   f) What is meant by transmission gate?
   g) Briefly explain about PLA.
   h) Write brief notes on gate arrays?
   i) What do you mean by DFT?
   j) What is the aim of adhoc test techniques?
   k) What is a pull down device?

PART – B

Answer any *THREE* questions. All questions carry equal marks.

3 x 16 = 48 M

2. a) Describe N-well process in detail. 10 M

   b) Explain the transfer characteristics of CMOS inverter with neat sketch. 6 M

3. a) Design a layout for CMOS logic for $Y = \overline{(A+B)(C+D)}$ 8 M

   b) Explain about sheet resistance and sheet capacitance. 8 M

4. a) Write the scaling factors for different types of device parameters. 10 M

   b) How switch logic can be implemented using Pass Transistors? 6 M

5. a) Design a BCD to excess-3 converter using PLA? 10 M

   b) Compare PLA,PAL,PROM and CPLD. 6 M

6. a) Explain the system level test techniques? 12 M

   b) Explain about different fault models in VLSI testing? 4 M